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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/777,902 | 02/13/2004 | Kenneth Koch II | 10017912-3 | 6091 |

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| EXAMINER | |
|---|---|
| NGUYEN, LONG T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/777,902 | KOCH ET AL. | |
| | Examiner | Art Unit | |
| | Long Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-9 and 11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/13/04 + 3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence(s) of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)). If the prior application is a non-provisional application, the specific reference must also include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

### *Specification*

2. The disclosure is objected to because of the following informalities: throughout the specification, references "28" and "30" are referred as "DC circuits". However, it is not clear how the references "28" and "30" can be "DC circuits" because it appears from the drawings of Figure 1 that each of the "28" and "30" are just a path or a wire. Further, it is also not clear how the "path" 28 and 30 can be "DC" because each of them has a voltage signal that transitions/swings between ground and supply Vdd. Note that "DC path" and "DC connections" throughout the specification are also objected to for the similar reasons and because it is not clear what it means by "DC connections". Clarification and/or appropriate correction is required.

### *Claim Objections*

3. Claims 3-6, 8, 9 and 14-21 are objected to because of the following informalities:

Claim 3, line 2, --of the opposite power supply terminals-- should be inserted after "terminal" so that the antecedent basis is clear.

Claim 4 is objected to because it include the informality of claim 3.

Claim 5, on line 4, "NFET second transistor" should be changed to either --NFET transistor-- or --second transistor--.

Claim 5, line 4, --of the opposite power supply terminals-- should be inserted after "terminal" so that the antecedent basis is clear.

Claim 6, line 2, it is suggested to changed "PFET, NFET" to --said PFET of said driver, said NFET of said driver-- so that the antecedent basis is clear and the PFET is not being confused with the PFET of the switchable capacitor.

Claim 8, line 2, it is suggested that --switchable-- should be inserted before "capacitor" so that the antecedent basis is clear.

Claims 14-21 are objected to because they include the informalities of claim 8.

Claim 9, line 3, --of the opposite power supply terminals-- should be inserted after "terminal" so that the antecedent basis is clear.

Claim 15, line 3, "devices" should be changed to --transistors-- to provide antecedent basis for later claims (for example, provide antecedent basis for "all of the field effect transistors" in claim 16).

Appropriate correction is required.

***Double Patenting***

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 3-9 and 11-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,753,708, claims 1-5 of U.S. Patent No. 6,759,880, and claims 1, 3, 7-12, 14, 16-18, 20-26 of copending U.S. Application No. 10/777,174. Although the conflicting claims are not identical, they are not patentably distinct from each other because they claim substantially the same embodiment of the invention, i.e., all the claim limitations of U.S. Patents 6,753,708 and 6,759,880, and copending U.S. Application No. 10/777,174 anticipate all the claim limitations of the instant application.

Note that the double patenting with the copending U.S. Application No. 10/777,174 is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 3-9 and 11-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, "a threshold level" on line 5 and "a threshold voltage" on line 15 cause the claim to be indefinite because it is not clear if they are the same or different threshold since a threshold voltage inherently must also having a threshold level. Clarification and/or appropriate corrections is required.

Claims 3-9 and 11-21 are indefinite because they include the indefiniteness of claim 1.

Also in claim 5, line 5, first and second occurrences "the PFET second transistor" is indefinite because "PFET second transistor" does not make sense since the second transistor of driver is the NFET, so it is not clear if first and second occurrences "PFET second transistor" are for the NFET transistor (i.e., second transistor) or for the PFET transistor (i.e., first transistor) or whether if any of them is for the PFET transistor of the at least one switchable capacitor. Further, if first and second occurrences "PFET second transistor" are for the PFET transistor (i.e., first transistor) then the recitation "comprises a PFET ... is on" recited on the last 4 lines of the claim is indefinite because it is not understood how the PFET switchable capacitor (34, which is connected between the gate of NFET 50 and VDD) is for supplying current to the source-drain path of PFET 48 transistor of the driver. Clarification and/or appropriate correction is requested.

Claim 6 is also indefinite because it includes the indefiniteness of claim 1.

In claim 14, "DC path" recited on lines 5 and 6 is indefinite because it is not clear how it is a "DC". It is seen in the operation of the circuitry in Figure 1 that each of the paths 28 and 30 having a voltage signal that transitions/swings between ground and power supply Vdd, which is not DC voltage.

Also in claim 7, the recitation "the power supply terminal" on line 4 is indefinite because it is not clear which power supply terminal of the opposite power supply terminals that it is

referred to. Further, the recitation "comprises an NFET ... is on" recited on the last 4 lines of the claim is indefinite because it is not understood how can the NFET switchable capacitor 32 (connected between the gate of the PFET 48 and ground) is for supplying current to the NFET (50, i.e., second transistor of the driver). Clarification and/or appropriate correction is requested.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 3-9, 11-17 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bui et al. (USP 6,201,752).

With respect to claim 1, Figure 8A discloses a circuit, which includes: a first terminal (801) for receiving a voltage source (IN); a driver (CMOS inverter 809) including first (PMOS inside CMOS inverter 809) and second (NMOS inside CMOS inverter 809) opposite conductivity type transistors, each includes a control electrode (gate) and a path (drain-source path) switched on and off in response to the control electrode being on opposite sites of a threshold, the first and second paths being connected in series across opposite power supply terminals (power voltage and ground of the circuitry); an output terminal (810); and circuitry (802, 803, 805, 806, 807, 808) including at least one switchable capacitor (807 or 808) connected as recited in claim 1. Note that the operation of Figure 8A also meets the functional limitations of the circuitry recited ion the last 9 lines of the claim.

With respect 3, Figure 8A shows the at least one switchable capacitor (807 or 808) connected between one of the control electrodes and a DC power supply terminal.

With respect to claim 4, Figure 8A shows the circuitry including at least one resistive element (either 803 or 805).

With respect to claim 5, Figure 8A shows the first and second transistors (PMOS and NMOS inside of inverter 809) are respectively a PFET and an NFET, and the at least one switchable capacitor (807) including a PFET having a first electrode (gate) connected to a gate electrode of the NFET transistor (NMOS inside inverter 809) of the driver and a second electrode connected to power supply.

With respect to claim 6, Figure 8A shows the resistive element (803 or 805) comprises a resistor, and the PFET and NFET of the driver, and the at least one switchable capacitor are included on an integrated circuit chip.

With respect to claim 7, Figure 8A shows the first and second transistors (PMOS and NMOS inside of inverter 809) are respectively a PFET and an NFET, and the at least one switchable capacitor (808) including an NFET having a first electrode (gate) connected to a gate electrode of the PFET transistor (NMOS inside inverter 809) of the driver and a second electrode connected to ground.

With respect to claim 8, Figure 8A shows the at least one switchable capacitor (807, 808) includes a first switchable capacitor (808) and a second switchable capacitor (807) respectively connected to the control electrodes of the first (PMOS transistor inside 809) and second (NMOS transistor inside 809) transistors.

With respect to claim 9, Figure 8A shows the first and second capacitors (808 and 807) respectively connected between the control electrodes of the first and second transistors (PMOS and NMOS inside of 809) and first and second power supply terminals (ground and power supply). Note the functional recitation regarding finite capacitance and open circuit recited on the last 5 lines of the claim is inherently met because the structures of the first and second capacitors (transistor connected capacitor) are similar as applicant's invention. Note that the first and second threshold voltages of the first and second capacitors, respectively, are different because the threshold for PMOS transistor is different from the threshold voltage for NMOS transistor.

With respect to claim 11, Figure 8 shows the circuitry including first and second resistive elements (805 and 803).

With respect to claim 12, Figure 8A shows the first and second transistors (PMOS and NMOS inside 809) are PFET and NFET (inside 809) and the first and second capacitors (808 and 807) are respectively an NFET (808) and a PFET (807).

With respect to claim 13, Figure 8A shows the first and second transistors, the first and second capacitors and the first and second resistive elements are included in an integrated circuit chip.

With respect to claim 14, Figure 8A shows the circuitry including a first inverter (802-803, because when input IN = Lo then 802-803 output a Hi, which is reasonable to be considered as an inverter), and a second inverter (805-806, because when input IN = Hi then 805-806 outputs a Lo which is also reasonable to be considered as an inverter) each having an input terminal (at the gate of 802 for the first inverter, and at the gate of 806 for the second inverter),

an output terminal (at the end of resistor 803 that connected to terminal 804 for the first inverter, and at the end of resistor 805 that also connected to terminal 804 for the second inverter), a first DC path (path through resistor 803) and a second DC path (path through resistor 805).

With respect to claim 15, Figure 8A shows the first and second transistors (PMOS and NMOS inside 809) are field effect transistors, the first and second inverters (802-803 and 805-806) comprise field effect transistors (802 and 806), and the first and second capacitors (808, 807) comprise field effect transistors.

With respect to claims 16-17, Figure 8A shows all the transistors are included on an integrated circuit chip, and including first and second resistors (803, 805) of the respective first and second inverters.

With respect to claims 22-24, Figure 8A shows a circuit including first and second opposite conductivity transistors (PMOS and NMOS transistors inside 809), opposite first and second power supply terminals (power voltage and ground), an output terminal (810), and first and second switchable capacitors (808 and 807) with the connections that meets all the structural limitations as discussed above with regard to the apparatus claims. Hence, the operation of Figure 8A meets all the method steps recited in claims 22-24.

10. Claims 1, 3, 4, 8 and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamasaki et al. (USP 5,694,065).

Note that Figure 2 of the Hamasaki et al. reference discloses a circuit having an input terminal (IN); voltage source (INPUT signal); a driver (50, 60) comprising first and second opposite conductivity type transistors (PFET and NFET, respectively); opposite power supply terminals (Vdd and ground); an output terminal (OUT); circuitry (70, 80); wherein the pulse

shaping circuitry (70, 80) including: (a) first and second inverters (IV1- Rn, IV2- Rp) each including an input terminal (terminal connected to input signal IN) and an output terminals (DO1 and DO2, respectively), and (b) first and second switchable capacitors (Cn) and (Cp); a first power supply terminal (power Vdd) and a second power supply terminal (ground); each of the first and second inverters including a PFET, an NFET and a resistor (i.e., the first inverter includes PFET 72, NFET 74 and resistor Rn, wherein the output of the first inverter is DO1, note Rn is connected between source drain path of the NFET 74 of the first inverter and the output DO1; and the second inverter including PFET 82, NFET 84 and resistor Rp wherein the output of the second inverter is DO2, and note that Rp is connected between source drain path of PFET 82 of the second inverter and the output DO1). Note that all the functional operations are met in the operation of the circuitry. Further, because the PFET and NFET transistors having opposite conductivity and because signals DO1 and DO2 having substantially same voltage level (i.e., signals DO1 and DO2 are inverted of input voltage signal IN), so the on/off of transistors 50 and 60 in Figure 2 must be opposite to each other, i.e., transistors 50 and 60 are not ON simultaneously. Thus, because the structure of the claims are fully met so the circuit in Figure 2 also capable of performs all of the functional limitations as the circuit of applicant's invention (MPEP 2114; In re Swinehart, 169 USPQ 226 (CCPA 1971); and In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997)).

***Allowable Subject Matter***

11. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims, and if amended to overcome the indefiniteness and informalities set forth above.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 5, 2005

LONG NGUYEN
PRIMARY EXAMINER